IN THE CLAIMS:

1. (Currently Amended) A phase locked loop device comprising:

a prescaler ~~for dividing~~ configured to divide the frequency of an output signal of the phase locked loop device by a prescaler factor, said prescaler being operable in at least two modes, each mode having assigned a different prescaler factor; and

an accumulator connected to said prescaler ~~for providing~~ configured to provide a mode switching signal to said prescaler to switch between said at least two modes having assigned different prescaler factors, said accumulator storing an accumulator value,

wherein said accumulator is adapted to repetitively update said accumulator value using a modulus function, to generate said mode switching signal to switch between said at least two modes having assigned different prescaler factors.

2. (Original) The phase locked loop device of claim 1, wherein said accumulator is connected to receive a tune parameter selected for tuning the frequency of said output signal, wherein said accumulator is adapted to take into account said tune parameter when processing the modulus function for generating said mode switching signal.

3. (Original) The phase locked loop device of claim 1, further comprising:

a divider unit connected to said prescaler for dividing the frequency of the prescaler output by a fixed divider factor, wherein said accumulator is adapted for processing said modulus function dependent on a received

modulus parameter, and said fixed divider factor is equal to said modulus parameter.

4. (Original) The phase locked loop device of claim 1, wherein said accumulator is adapted for taking into account a modulus parameter and receiving a tune parameter, the modulus parameter being a fixed divider factor of a divider unit of the phase locked loop device, the tune parameter being selected for tuning the frequency of said output signal, wherein said accumulator is adapted to take into account said modulus parameter and said tune parameter when processing the modulus function for generating said mode switching signal.

5. (Original) The phase locked loop device of claim 4, wherein said accumulator is adapted to calculate the sum of the accumulator value and the tune parameter and to calculate the accumulator value to be the result of applying said modulus function to said sum and said modulus parameter.

6. (Original) The phase locked loop device of claim 4, wherein said modulus parameter is hard coded in said accumulator.

7. (Original) The phase locked loop device of claim 1, wherein said accumulator comprises a plurality of subunits having reduced bit widths.

8. (Original) The phase locked loop device of claim 7, wherein the bit width of each subunit of said accumulator is three bits.

9. (Original) The phase locked loop device of claim 1, further comprising:

an input terminal for receiving a reference signal having a frequency to be compared with a frequency of a phase locked loop feedback signal for adjusting the frequency of said output signal.

10. (Original) The phase locked loop device of claim 9, wherein said accumulator is adapted for changing said mode switching signal at least three times in each period of said reference signal.

11. (Original) The phase locked loop device of claim 1, adapted for being operated in a transceiver of a WLAN (Wireless Local Area Network) communication system.

12. (Original) The phase locked loop device of claim 1, adapted for being operated as a frequency synthesizer.

13. (Currently Amended) An integrated circuit chip having a phase locked loop circuit, comprising:

a prescaler circuit ~~for dividing~~ configured to divide the frequency of an output signal of the phase locked loop circuit by a prescaler factor, said prescaler circuit being operable in at least two modes, each mode having assigned a different prescaler factor; and

an accumulator circuit connected to said prescaler circuit ~~for providing~~ configured to provide a mode switching signal to said prescaler circuit to switch between said at least two modes having assigned different prescaler factors, said accumulator circuit storing an accumulator value,

wherein said accumulator circuit is adapted to repetitively update said accumulator value using a modulus function, to generate said mode switching signal to switch between said at least two modes having assigned different prescaler factors.

14. (Currently Amended) A transceiver in a WLAN (Wireless Local Area Network) communication system, the transceiver having a phase locked loop device comprising:

a prescaler ~~for dividing~~ configured to divide the frequency of an output signal of the phase locked loop device by a prescaler factor, said prescaler being operable in at least two modes, each mode having assigned a different prescaler factor; and

an accumulator connected to said prescaler ~~for providing~~ configured to provide a mode switching signal to said prescaler to switch between said at least two modes having assigned different prescaler factors, said accumulator storing an accumulator value,

wherein said accumulator is adapted to repetitively update said accumulator value using a modulus function, to generate said mode switching signal to switch between said at least two modes having assigned different prescaler factors.

15. (Currently Amended) A method of operating a phase locked loop device, the method comprising:

dividing the frequency of an output signal of the phase locked loop device in a prescaler of said phase locked loop device by a prescaler factor, said prescaler being operable in at least two modes, each mode having assigned a different prescaler factor; and

generating a mode switching signal for changing the mode of said prescaler to another mode of said at least two modes having assigned different prescaler factors,

wherein generating the mode switching signal comprises:

storing an accumulator value; and

processing a modulus function for updating said accumulator value.

16. (Original) The method of claim 15, wherein the step of processing said modulus function comprises:

receiving a tune parameter for tuning the frequency of said output signal.

17. (Original) The method of claim 15, wherein the step of dividing the frequency of said output signal comprises:

dividing the frequency of a prescaler output by a fixed divider factor;

wherein processing said modulus function depends on a received modulus parameter,

wherein said fixed divider factor is equal to said modulus parameter.

18. (Original) The method of claim 15, wherein the step of processing said modulus function comprises:

receiving a modulus parameter and a tune parameter, said modulus parameter being a fixed divider factor and said tune parameter being selected for tuning the frequency of said output signal, and

taking into account said modulus parameter and said tune parameter when updating said accumulator value.

19. (Original) The method of claim 18, wherein the step of processing said modulus function further comprises:

calculating a sum of said accumulator value and said tune parameter, and calculating said updated accumulator value to be the result of applying said modulus function to said sum and said modulus parameter.

20. (Original) The method of claim 19, wherein the step of calculating further comprises:

storing said sum as the updated accumulator value in a register.

21. (Original) The method of claim 19, wherein the step of calculating said sum comprises:

subtracting said modulus parameter from said sum, and

storing the difference as the updated accumulator value in a register.

22. (Original) The method of claim 21, wherein further comprising:

comparing said sum with said modulus parameter,

wherein calculating the updated accumulator value comprises:

changing the mode switching signal such that said prescaler changes its mode depending on the comparing result.

23. (Original) The method of claim 15, further comprising:

receiving a reference signal having a frequency to be compared with a frequency of a phase locked loop feedback signal, and

adjusting the frequency of said output signal.

24. (Original) The method of claim 23, wherein the step of adjusting comprises:

changing said mode switching signal at least three times in each period of said reference signal.

25. (Original) The method of claim 15, adapted for operating said phase locked loop device in a transceiver of a WLAN (Wireless Local Area Network) communication system.

26. (Original) The method of claim 15, further adapted for operating said phase locked loop device as a frequency synthesizer.